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The time period for reply, if any, is set in the attached communication.

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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/661,037
Filing Date: September 12, 2003
Appellant(s): HYDE ET AL.

Thomas Van Zandt
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed June 7, 2007 appealing from the Office action mailed August 24, 2006.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| **6,563,731** | **Bergemont** | **5-2003** |
| **6,777,758** | **Yamashita et al.** | **8-2004** |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 36-37, 39-40, 44-49 and 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergemont (US 6,563,731 B1) in view of Yamashita et al. (US 6,777,758 B2).

In regard to claims 36, 38, 44-48 and 50, Bergemont teaches a p-channel floating gate device, comprising: a p- doped substrate 202; a first n- well (to the left of well 205) and a second n- well 205 disposed in the substrate 202; a first p+ doped region disposed in the first n- well (to the left of well 205) forming a source and a second p+ doped region disposed in the first n- well (to the left of well 205) forming a drain; a channel disposed in the first n-well (to the left of well 205) between the source and the drain; a tunneling junction in the second n- well 205; a layer of gate oxide disposed above the channel, the first n- well (to the left of well 205) and the second n- well 205; a polysilicon (abstract) floating gate 204 disposed above the layer of gate oxide; a source contact terminal $V_{pp}$ electrically coupled to the source 206; a drain contact terminal $V_{pp}$ electrically coupled to the drain 207 (Figure 3, columns 4-5, lines 30-67 and 1-17, respectively).

In regard to claim 44 concerning the synapse transistor configured to operate as a current source without gate input using a single polysilicon gate layer, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than

function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the preamble of claims 45 and 47, the main body of the claims is taught by the applied reference above.

In regard to claims 39 and 51, Bergemont teaches the transistor formed with a single layer 204 of conductive polysilicon (abstract) (Figure 3, columns 4-5, lines 30-67 and 1-17, respectively).

In regard to the preamble, If the body of a claim fully and intrinsically sets forth all of the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction. Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999). See also Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997) ("where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention, the preamble is not a claim limitation").7

However, Bergemont fails to teach a well contact terminal coupled to a second n-well.

In regard to claims 36, 38 and 50, Yamashita et al. teach a well contact terminal 32 coupled to a second n- well 12 (Figure 1, columns 7-8, lines 1-67 and 1-67, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the transistor structure as taught by Bergemont with the transistor structure having a well contact terminal coupled to a second n- well as taught by Yamashita et al. to reduce the layout area of elements for fixing the potentials of wells in a semiconductor device (column 1, lines 6-10).

In regard to claims 37-38 and 49-50, Yamashita et al. teach the third p+ doped region and the fourth doped region disposed in a second well 12 p+ doped region shorted together with a conductive layer 40 which forms a bridge over a floating gate 62 (Figure 1, columns 7-8, lines 1-67 and 1-67, respectively).

In regard to claim 51, Yamashita et al. teach the well contact terminal 32 being strapped to a third and fourth doped region (Figure 1, columns 7-8, lines 1-67 and 1-67, respectively).

In regard to claims 40 and 52, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorne et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof

in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113.

**(10) Response to Argument**

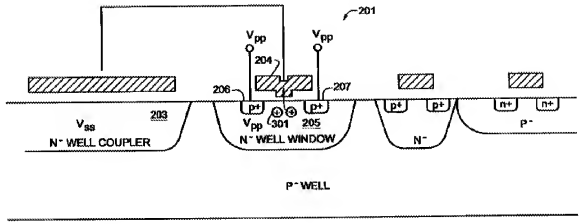


Figure 3

In regard to the remarks on page 15 of the Appeal Brief, the Examiner misstated as to which side of the second n- well 205 the first n- well was located (Bergemont [US 6,563,731 B1] Figure 3). Clearly what was meant was that the first p+ doped region is disposed in the first n- well, which is the n- well to the right (not left) of the second n- well 205. The n- well to the left of second n- well 205 has no p+ doped region. The Applicant is liable for the entire reference as a whole. In addition to the first n- well having a first p+ doped region the other claimed features relating to the first n-well, such as a channel (between the p+ doped regions), a source (left p+ doped region), a drain

(right p+ doped region) and source & drain contact terminals (inherent in the device or that particular transistor will not function).

Concerning the remarks on page 16 that Bergemont (US 6,563,731 B1) and Yamashita et al. (US 6,777,758 B2) are not combinable in regard to the processing differences and differences in the stated goals for achieving the products, both references are gate insulated field effect transistors having multiple wells. Bergemont and Yamashita et al. are in the same field of endeavor. That field of endeavor being gate-insulated semiconductor devices. The final structure of the references was combined to teach the final structure of the claimed invention, not the processes to fabricate the final structure of the references or the goals of achieving structures.

In regard to the remarks that reducing the layout is always a desired goal in any semiconductor device, In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the proof is in Yamashita et al. (Figure 1, columns 7-8, lines 1-67 and 1-67, respectively) as admitted by the applicant.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Ida M Soward/
Primary Examiner, Art Unit 2822

Conferees:

/N. Drew Richards/

Supervisory Patent Examiner, Art Unit 2895

Darren Schuberg /DS/

TQAS, TC 2800